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| EXAMINER | |
|---|---|
| KERVEROS, JAMES C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2138 | |

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/063,472 | OZAKI, HIDEHARU | |
| | Examiner | Art Unit | |
| | JAMES C. KERVEROS | 2138 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *5-20,25-29,31 and 33-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,21-24,30,32,37 and 38* is/are rejected.

7)☐ Claim(s) ____ is/are objected to.

8)☐ Claim(s) ____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/8/2004
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## FINAL OFFICE ACTION

This is a FINAL Office Action in response to AMENDMENT filed 2/2/2006, which is in reply to the prior Final Office Action dated 10/31/2005.

Applicant's request for reconsideration of the finality of the rejection of the last Office action dated 10/31/2005 is persuasive and, therefore, the finality of that action is withdrawn. New Claims 37 and 38 added in the Amendment dated September 20, 2005, have not been examined due to Examiner's over-sight. Therefore, a new FINAL Office Action is set forth, including the examination of Claims 37 and 38.

Claims 1-38 are pending in the application. Claims 5-20, 25-29, 31 and 33-36 having been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species. Claims 1-4, 21-24, 30, 32, 37 and 38 have been elected for examination.

### *Response to Arguments*

Applicant's arguments filed 2/2/2006, with respect to claims 1-4, 21-24, 30, 32, 37 and 38 have been fully considered but they are not persuasive.

Regarding independent Claim 1, Applicant argues, that in generating the two clock pulses 310a and 310b, in the Peng reference, the falling edge of CTL 112, the rising edge of TCK 110 and the two clock pulses 310a and 310b occur at almost the same time, and as such the falling edge of CTL 112 and rising edge of TCK 110 generates noise, which may influence the measurement of the delay test.

In response to Applicant's argument, the Examiner notes that Applicant's assertion of noise generation is based on pure speculation, since Peng discloses a

phase-lock-loop system, which precisely avoids the problems associated with noise generation, glitches or other undesired clock pulses. In the Summary of the Invention, Peng describes that the phase-lock-loop system clock, clock control and burst control logic are synchronized with the TCK signal. In this way, the TCK controls all cycle functions synchronously so that only two system clocks are applied to the device logic circuits during the input cycle. Even though the phase-lock-loop is running continuously, the test/normal control signal and TCK control all test functions without glitches or other undesired clock pulses. A feature of the present invention is utilizing two high speed clock pulses that are synchronized with the test system clock so that precise and repeatable control of the logic test occurs.

In response to Applicant's argument above, Peng describes, "in the test mode, voltage controlled oscillator clock 204 is phase-locked to the frequency of TCK 110. This allows synchronous glitch free operation during the scan-path test cycles because every event during a cycle, and each cycle change, occurs on a positive edge of the TCK 110. Setup and settling transitions do not create false signals nor glitches because they occur during the time TCK 110 is at a low logic level. Thus, all logic control during the test mode is dependant on and in time sync with the logic levels of TCK 110" (Col. 6, lines 1-8).

Further, in response to Applicant's argument above, Peng describes, "The clock pulses 312 and 316 are phase locked in frequency and phase, therefore each clock pulse leading edge, when going from a logic low to a logic high, will occur at substantially the same time as is indicated by the number 318. When TCK 110 goes

from logic low to logic high, during input cycle 308, the burst controller 208 allows only two clock pulses 310a and 310b to pass through. The clock pulses 310a and 310b are derived from the clock pulses 312 of SCK-1 222" (Col. 7, lines 45-55).

In response to Applicant's argument that Peng fails to anticipate "generating a gate signal after a predetermined interval as measured from an input timing of a control signal", as recited in claim 1, clearly, such a limitation fails to overcome the prior art of record, since Peng generates the two clock pulses 310a and 310b in synchronization with the clock pulses 312 and 316, which are phase locked in frequency and phase, and therefore each clock pulse leading edge, when going from a logic low to a logic high, will occur at substantially the same time as is indicated by the number 318, thus avoiding the need of a gate signal.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 37, 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Peng (U.S. Patent No. 5,524,114), issued: June 4, 1996.

Regarding independent Claim 1, Peng discloses a semiconductor die test jig 104 for holding and probing a semiconductor integrated circuit die or dice 202 having a test

circuit including scan-path logic 214, VCO 204, phase detector 206, frequency divider 210, and burst controller 208 to enable scan-path delayed ATPG testing of the combinational logic 212, (Figures 1, 2 and 3), comprising:

A two-pulse generator (burst controller 208) for generating two clock pulses (310a and 310b) spaced from each other by a pulse interval equal to a period of a test clock (SCK-1) 222, which is originated from an external source (VCO 204), where the clock pulses 310a and 310b are applied as G-SCK-1 224 to the combinational logic 212 at time 318 which begins the scan-path data test of the combinational logic 212. The first clock pulse 310a causes the combinational logic 212 to start processing the scan-path data, and the second clock pulse 310b to stop the data processing,

Wherein the two-pulse generator (burst controller 208) comprises:

A gate signal generator, such as the burst controller 208 is utilized to "gate off and control the number of clock pulses to the combinational logic 212 during testing" (col. 6, lines 10-15), by gating signals CTL 112 and TCK 110 with SCK-1 222, the burst controller 208 allows only two clock pulses 310a and 310b to pass through. The clock pulses 310a and 310b are derived from the clock pulses 312 of the test clock SCK-1 222, Figure 3.

Regarding Claim 2, Peng discloses the test circuit of claim 1 is fabricated in the semiconductor integrated circuit die or dice 202 and further comprises:

A PLL circuit (phase-lock-loop) formed by the VCO 204, frequency divider 210 and phase detector 206 for synchronizing the frequency and phase of the internal clock output 222 to the frequency and phase of TCK 110, and using the modulo-N frequency

divider 210 for dividing the clock output 222 frequency by a divide ratio N and then supplying the test clock output 222 to the two-pulse generator (burst controller 208). It is noted that dividing the clock output 222 by N is the equivalent of multiplying the clock output 222 by 1/N (col. 5, lines 51-62). The PLL circuit (phase-lock-loop) is part of the test circuit, which is fabricated in the semiconductor integrated circuit device (die or dice 202) Figure 2.

Regarding Claims 37, 38, Peng discloses a gate signal generator (burst controller 208) utilized to "gate off and control the number of clock pulses to the combinational logic 212 during testing" (col. 6, lines 10-15), by gating signals CTL 112 and TCK 110 with SCK-1 222, the burst controller 208 allows only two clock pulses 310a and 310b to pass through. The clock pulses 310a and 310b are derived from the clock pulses 312 of the test clock SCK-1 222, Figure 3.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 4, 21-24, 30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peng (U.S. Patent No. 5,524,114) in view of Conner (U.S. Patent No. 5,794,175).

Regarding Claim 3, Pen substantially discloses the claimed invention as applied to claims 1 and 2 above. Peng does not explicitly disclose a test circuit mounted on a test board and a semiconductor integrated circuit device removably mounted on the test board. However, Peng discloses a semiconductor die test jig 104, corresponding to a PCB test board, for holding and probing a semiconductor integrated circuit die or dice 202 having a test circuit, Figure 1 and 2. Furthermore, in analogous art, Conner discloses a printed circuit board (PCB) Memory array board 210 having sockets for inserting integrated circuits, DUTs 116, for burn-in quality testing. The Memory array board 210 also includes a test fan out circuitry 214 that controls the provision of data from the devices under test 116 to error processor 124, (Figure 2, Conner).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to mount sockets and a test circuit as taught by Conner on the semiconductor die test jig 104 of Peng for the purpose of inserting numerous memory chips into the sockets for burn-in quality testing, since sockets are well known in the art for providing flexibility, by removing or inserting chips during various testing stages. For example, following burn-in, the memory chips are generally removed from the burn in board and passed to a test stage where a more complete test is performed. Further motivation in using a test board with sockets is a result of some manufacturing operations, where memory devices are inserted into a burn-in board and the same

board could be used for burn in and for holding memory devices for test, where the memory devices are passed directly from the burn-in stage to the test stage on the same printed circuit boards, and then memory devices are removed for final packaging upon completion of testing, thus reducing the number of transfer steps that are required during the semiconductor manufacturing operation, which can increase throughput and reduce cost (Col. 9, lines 57-67, Conner).

Regarding Claim 4, Peng discloses a PLL circuit (phase-lock-loop) formed by the VCO 204, frequency divider 210 and phase detector 206 for synchronizing the frequency and phase of the internal clock output 222 to the frequency and phase of TCK 110, and using the modulo-N frequency divider 210 for dividing the clock output 222 frequency by a divide ratio N and then supplying the test clock output 222 to the two-pulse generator (burst controller 208). It is noted that dividing the clock output 222 by N is the equivalent of multiplying the clock output 222 by 1/N (col. 5, lines 51-62). The PLL circuit (phase-lock-loop) is fabricated in the semiconductor integrated circuit device (die or dice 202) Figure 2.

Regarding Claim 21, Peng substantially discloses a clock generator (VCO 204) for outputting the test clock (SCK-1) 222. Peng does not explicitly disclose a test board on which a semiconductor integrated circuit device is removably mounted. However, Peng discloses a semiconductor die test jig 104, corresponding to a PCB test board, for holding and probing a semiconductor integrated circuit die or dice 202 having a test circuit, Figure 1 and 2. Furthermore, in analogous art, Conner discloses a printed

circuit board (PCB) Memory array board 210 having sockets for inserting integrated circuit, ICs, DUTs 116, for burn-in quality testing (Figure 2, Conner).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to mount sockets as taught by Conner on the semiconductor die test jig 104 of Peng for the purpose of inserting numerous memory chips into the sockets during burn-in quality testing, since sockets are well known in the art for providing flexibility, by removing or inserting chips during various testing stages. For example, following burn-in, the memory chips are generally removed from the burn in board and passed to a test stage where a more complete test is performed. Further motivation in using a test board with sockets is a result of some manufacturing operations, where memory devices are inserted into a burn-in board and the same board could be used for burn in and for holding memory devices for test, where the memory devices are passed directly from the burn-in stage to the test stage on the same printed circuit boards, and then memory devices are removed for final packaging upon completion of testing, thus reducing the number of transfer steps that are required during the semiconductor manufacturing operation, which can increase throughput and reduce cost (Col. 9, lines 57-67, Conner).

Regarding Claims 22, 32, Peng substantially discloses the claimed invention as applied to claim 1, above. Peng does not explicitly disclose a frequency divider mounted on the test board for dividing the frequency of the test clock into a frequency, which can easily be measured. However, Peng discloses a modulo-N frequency divider 210 for dividing the clock output 222, located in the semiconductor integrated circuit die or dice

202, which is mounted on the semiconductor die test jig 104. Furthermore, in analogous art, Conner discloses a test fan out circuitry 214, which is mounted on a printed circuit board (PCB) Memory array board 210 (Figure 2, Conner).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to mount a test circuit, as taught by Conner, such as a modulo-N frequency divider 210 on the semiconductor die test jig 104 of Peng, for the purpose of performing test clock measurements at lower frequencies with respect to the operating frequency, since both Peng and Conner disclose standard testers that operate at low frequencies.

Regarding Claim 23, Peng substantially discloses a clock generator (VCO 204) for outputting the test clock (SCK-1) 222, wherein the two-pulse generator (burst controller 208) is fabricated in the semiconductor integrated circuit die or dice 202. Peng does not explicitly disclose a semiconductor integrated circuit device, which is removably mounted to a test board, and a clock generator mounted on the test board. However, Peng discloses a semiconductor integrated circuit die or dice 202, which is mounted on the semiconductor die test jig 104, and where the clock generator (VCO 204) is located in the semiconductor die test jig 104. Furthermore, in analogous art, Conner discloses a printed circuit board (PCB) Memory array board 210 having sockets for inserting integrated circuit, ICs, DUTs 116, for burn-in quality testing. The Memory array board 210 also includes a test fan out circuitry 214 that controls the provision of data from the devices under test 116 to error processor 124, (Figure 2, Conner).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to mount sockets and a test circuit, as taught by Conner, such as a VCO 204 on the semiconductor die test jig 104 of Peng for the purpose of inserting numerous memory chips into the sockets during burn-in quality testing, since sockets are well known in the art for providing flexibility, by removing or inserting chips during various testing stages. For example, following burn-in, the memory chips are generally removed from the burn in board and passed to a test stage where a more complete test is performed. Further motivation in using a test board with sockets is a result of some manufacturing operations, where memory devices are inserted into a burn-in board and the same board could be used for burn in and for holding memory devices for test, where the memory devices are passed directly from the burn-in stage to the test stage on the same printed circuit boards, and then memory devices are removed for final packaging upon completion of testing, thus reducing the number of transfer steps that are required during the semiconductor manufacturing operation, which can increase throughput and reduce cost (Col. 9, lines 57-67, Conner).

Regarding Claim 24, Peng discloses a PLL circuit (phase-lock-loop) formed by the VCO 204, frequency divider 210 and phase detector 206 for synchronizing the frequency and phase of the internal clock output 222 to the frequency and phase of TCK 110, and using the modulo-N frequency divider 210 for dividing the clock output 222 frequency by a divide ratio N and then supplying the test clock output 222 to the two-pulse generator (burst controller 208). It is noted that dividing the clock output 222 by N is the equivalent of multiplying the clock output 222 by 1/N (col. 5, lines 51-62).

The PLL circuit (phase-lock-loop) is fabricated in the semiconductor integrated circuit device (die or dice 202) Figure 2. Wherein, the PLL circuit (phase-lock-loop) is fabricated in the semiconductor integrated circuit device (die or dice 202) Figure 2.

Regarding Claim 30, Peng substantially discloses a PLL circuit (phase-lock-loop) formed by the VCO 204, frequency divider 210 and phase detector 206 for synchronizing the frequency and phase of the internal clock output 222 to the frequency and phase of TCK 110, and using the modulo-N frequency divider 210 for dividing the clock output 222 frequency by a divide ratio N and then supplying the test clock output 222 to the two-pulse generator (burst controller 208). It is noted that dividing the clock output 222 by N is the equivalent of multiplying the clock output 222 by 1/N (col. 5, lines 51-62). The PLL circuit (phase-lock-loop) is fabricated in the semiconductor integrated circuit device (die or dice 202) Figure 2.

Peng does not explicitly disclose a second PLL circuit mounted on the test board. However, in analogous art, Conner discloses a test fan out circuitry 214, which is mounted on a printed circuit board (PCB) Memory array board 210 (Figure 2, Conner).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to mount a test circuit, as taught by Conner, such as a second PLL circuit on the semiconductor die test jig 104 of Peng, for the purpose of generating a clock at lower frequencies with respect to the operating frequency, since both Peng and Conner disclose standard testers that operate at low frequencies.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

By: 2/16/06

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PRIMARY EXAMINER

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